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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/525,603	11/10/2005	Hiroshi Miyagi	A-490	7954

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EXAMINER	
JOHNSON, RYAN	

ART UNIT	PAPER NUMBER
2817	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/525,603	MIYAGI ET AL.	
	Examiner	Art Unit	
	Ryan J. Johnson	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 9-15* is/are rejected.

7)☒ Claim(s) *7 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 February 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/22/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☒ Other: *Machine translations of '554 and '038.*

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the power supply voltage and temperature detectors (see claims 7 and 8) must be shown (see Fig.1) or the feature(s) canceled from the claim(s). Furthermore, the non-volatile memory (see claim 6) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New

Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claim 5 is objected to because of the following informalities: "the values of the bits" lacks antecedent basis (see line 5 of claim 5). The Examiner suggests using the recitation, "values of the bits". Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 4, 12 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Claim 4 recites "the capacitance mutually". It is unclear what particular capacitance is being referred to as "the capacitance mutually". The Examiner suggests adopting the language, "characterized in that the plurality of second capacitors are binary weighted".

7. Claims 12 and 14 recite, "the plurality of second capacitors" (see lines 10-11 of claim12 and lines 8-9 of claim 14). However, there is no "plurality of second capacitors" recited within claim 1. The Examiner suggests amending these claims to be dependent upon claim 2 rather than claim 1, and for the purpose of applying art, the Examiner is interpreting claims 12 and 14 to be dependent upon claim 2 rather than claim 1.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 9, 10, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori (Japanese Publication No. 06-291554, as cited by applicant and hereinafter "Mori") in view of Emura et al. (Japanese Publication No. 11-55038, as cited by applicant and hereinafter "Emura").

10. The Examiner notes machine translations of each pertinent Japanese reference discussed herein are provided with the present action and are referenced in the following discussions.

11. Regarding independent claim 1, Mori discloses a receiver (see Figs.1,3) comprising a detector (Figs.1,3) of which characteristic values are varied by adjusting a capacitance value (of varactor 25), characterized in that:

the detector comprises a variable capacitance circuit (25) formed on a and a resonance circuit (21, 22, 24) composed of an inductor (24) and a first capacitor (21); and

the characteristic values of the detector are adjustable by varying the capacitance value of the variable capacitance circuit (see [0014], which discusses adjusting the characteristics of the phase shifter by varying capacitance 25).

12. The difference between the recited invention and Mori lies with the physical arrangement of circuit components, of which Mori does not discuss. The recited invention requires a variable capacitance circuit formed on a semiconductor substrate with the resonance circuit formed outside the semiconductor substrate (i.e. external to the circuit where the variable capacitance resides). Emura discloses a similar phase shift circuit in a similar FM recovery circuit (see Figs.5,6), where the resonant circuit is external to the chip in which the remainder of circuitry resides (see [0007] of Emura). It is common within the art to provide resonators external to other circuitry in a manner discussed in Emura, in part due to the difficulty in integrating inductors of appropriate sizes within an integrated circuit. Furthermore, the recited physical arrangement of circuit components is a matter of design choice, as there is no discernable difference of circuit operation with the resonator located external to the variable capacitance circuit. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided the resonator circuit of Mori external to a substrate in which the remainder of the components are located, as disclosed by Emura, in order to have provided a suitable design choice alternative.

13. Regarding claim 9, Mori discloses the detector as a quadrature detector (see [0001]) having a pi/2 phase shifter (see paragraph [0004], which discusses the phase shifter 2 shifting by 90 degrees, and paragraph [0013], which discusses the phase converter operating identically, i.e. with a 90 degree phase shift, but with a variable capacitance rather than inductor) comprised of the resonance circuit (21,22,24) and variable capacitance circuit (25) and the capacitance of the variable capacitor (25) is

adjusted to provide an optimum 90 degree phase shift against the input signal (see [0016]).

14. Regarding claims 10 and 11, although Mori does not explicitly disclose a semiconductor substrate with other components formed thereon or formed using a CMOS or MOS process, the Examiner takes Official Notice that integrating numerous circuit components on a semiconductor substrate is well known and well documented within the art and provides the benefits of reduced package size.

15. Claims 2-5, 12, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori in view of Emura as applied to claim 1 above, and further in view of Nystrom et al. (U.S. Patent No. 6,686,809, hereinafter "Nystrom").

16. Regarding claim 2, Mori and Emura disclose the limitations of claim 1, as discussed in greater detail above. The difference between Mori/Emura and the recited invention of claim 2 lies with the variable capacitance. Mori discloses a varactor tuned via an analog voltage, while the recited invention requires a plurality of second capacitors and switches for connecting the capacitors in parallel. Nystrom discloses a phase shifter apparatus (see Fig.3) that utilizes switched capacitances (C_{20} - C_{23}, switched with switches S_{20} - S_{23}) rather than the single analog varactor of Mori. The Examiner notes a benefit of using such switched capacitances includes a greater tuning range and compatibility with digital control. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have implemented

the switched capacitive structure of Nystrom in place of the analog varactor of Mori in order to have provided the benefits of increased tuning range and digital compatibility.

17. Regarding claims 3 and 4, Mori and Emura do not explicitly disclose the recited second capacitances, as discussed above. Nystrom discloses the second switched capacitances, and also discloses said switched capacitances as different from one another and set at twice the capacitance mutually (i.e., the capacitances are binary-weighted; see col.5,25-32). The Examiner notes that such binary-weighting provides the benefits of balanced range and resolution, as well as increased digital compatibility. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have implemented binary weighting along with the switched capacitances of Nystrom in place of the analog varactor of Mori in order to have provided the benefits of balanced range and resolution as well as increased digital compatibility.

18. Regarding claim 5, Mori discloses a storage unit (28) for storing data corresponding to the varactor capacitance (see paragraphs [0017] and [0018]). In the combination of Mori, Emura, and Nystrom, one of skill in the art would have recognized the value stored in the memory corresponding to the A/D value (i.e. the digital output of 27) as a suitable signal for controlling the switches of a switches capacitance circuit (i.e. disclosed by Nystrom).

19. Regarding claims 12 and 14, Mori discloses inputting a test signal to the receiver (the input signal supplied to multiplier 1 and phase shifter 2 via 7 can be considered a "test" signal since it is actively used to adjust the phase shifter characteristics),

measuring the receiving state of the receiver (via voltage meter 4) and determining the receiving state of the receiver based on the measurement result (via A/D converter 5 and CPU 27) to optimize the variable capacitance (see [0017]-[0021], which describes the measurement and compensation operations via components 4, 5, 28, 27, 26, and 25). The Examiner notes that in the combination of Mori/Emura and Nystrom, the CPU would control the switched capacitance structure directly, as discussed in greater detail above (see paragraph 16 above).

20. Claims 6, 13, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori in view of Emura and Nystrom as applied to claims 1, 2, and 5 above, and further in view of Mattisson et al. (U.S. Patent No. 6,188,275, hereinafter "Mattisson"). Mori, Emura, and Nystrom disclose the limitations of claims 1, 2, and 5, as discussed in greater detail above. Mori also discloses the measuring and adjusting devices, as discussed in greater detail above (see paragraph 17). Mori also discloses the recited control unit (27) for storing data in the storage unit (28). While Mori does not explicitly disclose the recited "nonvolatile memory", the Examiner notes that registers, a form of nonvolatile memory, are common within CPUs, and using such registers to hold data during processing is well known and well documented in the art.

21. The most significant difference between the recited invention and claims 6, 13, and 15 lies with "optimizing a receiving state measured in advance" and storing data "before starting a receiving operation". In the circuit of Mori, all compensation is performed while the device is receiving information, rather than before a receiving

operation, as recited. Mattisson, however, discloses the use of a test signal (18b) for compensation while the receiver is not receiving a signal (see col.2,45-52). An easily recognizable benefit of such a system is the capability of keeping a system tuned even while not receiving a signal, thus ensuring an always-tuned system. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have implemented a separate test signal, as disclosed by Mattisson, in periods before a receiving operation in order to have provided the benefits of a system that is always properly tuned.

Allowable Subject Matter

22. Claims 7 and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

23. The following is a statement of reasons for the indication of allowable subject matter: the detection of temperature or a power supply voltage and subsequent varying of the contents of the data stored in the storage unit could not be found in the prior art within the context of the overall claims.

Conclusion

24. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Madsen (U.S. Patent No. 5,453,714) discloses a similar variable phase shifter in a similar demodulator (see Fig.5) comprising a variable capacitances (see Fig.6A).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan J. Johnson whose telephone number is (571)270-1264. The examiner can normally be reached on Monday - Friday, 9:00 am - 5:00 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert J. Pascal can be reached on 571-272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/R. J. J./
Examiner, Art Unit 2817

/Robert Pascal/
Supervisory Patent Examiner, Art Unit 2817